AMENDMENTS TO THE CLAIMS

1. (previously amended) A fast data access circuit, having a standard clock input signal, comprising:

a clock delay circuit that generates a delayed clock signal, from a plurality of selectable time delays, in response to the standard clock input signal and a delay control signal;

a control circuit that generates a mode control signal and the delay control signal;

a multiplexing circuit having a first input coupled to the standard clock input signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock in response to the mode control signal; and

a data output register, coupled to the multiplexing circuit and an input data bit, for outputting the input data bit in response to the selected clock.

2. (Original) The circuit of claim 1 wherein the data output register is a data first-in-first-out (FIFO) register.

3. (Original) The circuit of claim 2 and further including data FIFO register control logic, coupled between the multiplexing circuit and the data FIFO register, for generating FIFO control signals in response to the selected clock.

4. (Original) The circuit of claim 1wherein the control circuit comprises a mode/configuration register that generates the mode control signal in response to a loaded configuration word.

5. (Original) The circuit of claim 4 wherein the loaded configuration word is in response to a frequency of the standard clock input signal.

6. (Original) The circuit of claim 4 wherein the selectable time delay is selected in response to the loaded configuration word.

7. (Original) The circuit of claim 1 wherein the input data bit is part of a data stream from a memory array.

8. (Previously Amended) A fast data access circuit having an input clock signal and an input data signal, the circuit comprising:

a mode/configuration register for generating a mode control signal in response to a loaded configuration word;

a clock delay circuit coupled to the input clock signal and the mode/configuration register, the clock delay circuit providing, in response to the loaded configuration word, a selectable time delay, from a plurality of time delays, to the input clock signal to produce a delayed clock signal;

a multiplexing circuit having a first input coupled to the input clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal;

control logic for generating a plurality of register control signals in response to the selected clock signal; and

a data output register, coupled to the control logic and an input data bit, for outputting the input data bit in response to the register control signals.

9. (Original) The circuit of claim 8 wherein the loaded configuration word comprises at least one bit indicating a frequency of the input clock signal.

10. (Original) The circuit of claim 8 wherein the configuration word comprises at least one bit indicating a fast access mode or a standard mode.

11. (Original) A fast data access circuit having an input clock signal and an input data burst signal comprising a plurality of data bits, the input clock signal having a frequency, the circuit comprising:

a mode/configuration register for generating a mode control signal in response to a loaded configuration word comprising at least one mode control bit and at least one clock frequency selection bit that is set in response to the input clock signal frequency;

a clock delay circuit coupled to the input clock signal and the mode/configuration register, the clock delay circuit providing, in response to the at least one clock frequency selection bit, a selectable time delay to the input clock signal to produce a delayed clock signal such that the time delay is smaller for higher input clock signal frequencies;

a multiplexing circuit having a first input coupled to the input clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal;

control logic for generating a plurality of register control signals in response to the selected clock signal; and

a data first-in-first-out register, coupled to the control logic and the input data burst signal, for outputting each of the plurality of data bit in response to the plurality of register control signals.

12. (Original) The circuit of claim 11 wherein the clock delay circuit comprises a plurality of delay circuits each coupled to a selection circuit, each selection circuit being coupled to the at least one clock frequency selection bit.

13. (Original) The circuit of claim 12 wherein each of the plurality of delay circuits comprises a plurality of inverter gates.

14. (Previously Amended) A memory device comprising:

an array of memory cells for storing a plurality of data bits;

a clock input for accepting a clock signal; and

a fast data access circuit comprising:

a clock delay circuit that generates a delayed clock signal, from a plurality of selectable time delays, in response to the clock signal and a delay control signal;

a control circuit that generates a mode control signal and the delay control signal;

a multiplexing circuit having a first input coupled to the clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal; and

a data output register, coupled to the multiplexing circuit and the array of memory cells, for outputting the plurality of data bit at a data rate determined by the selected clock signal.

15. (Original) The memory device of claim 14 and further including a burst counter for generating a plurality of sequential addresses, within a predetermined address range, to the array of memory cells such that a plurality of data is accessed within the predetermined address range.

16. (Original) The memory device of claim 14 and further including data output register control logic that generates a plurality of data output register control signals from the selected clock signal.

17. (Original) The memory device of claim 16 wherein the data rate is determined by the data output register control signals.

18. (Previously Amended) An electronic system comprising:

a processor that generates control signals; and

a memory device for storing and accessing data in response to the control signals, the device comprising:

an array of memory cells for storing a plurality of data bits;

a clock input for accepting a clock signal; and

a fast data access circuit comprising:

a clock delay circuit that generates a delayed clock signal, from a plurality of selectable time delays, in response to the clock signal and a delay control signal;

a control circuit that generates a mode control signal;

a multiplexing circuit having a first input coupled to the clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal; and

a data output register, coupled to the multiplexing circuit and the array of memory cells, for outputting the plurality of data bit at a data rate determined by the selected clock signal.

19. (Previously Amended) A method for performing fast data access in a memory device comprising an array of memory cells, the method comprising:

generating a delayed clock signal from an input clock signal such that the delay is selected from a plurality of delays in response to a control input;

selecting between the input clock signal and the delayed clock signal to generate a selected clock signal;

generating a plurality of data output register control signals in response to the selected clock signal;

storing a plurality of data bits from the array of memory cells to a data output register; and

accessing the plurality of data bits from the data output register at a rate determined by the plurality of data output register control signals.

20. (Original) The method of claim 19 wherein the control input is a configuration word loaded into a mode/configuration register.

21. (Original) The method of claim 19 and further comprising receiving a configuration word comprising at least one bit indicating a fast data access mode and at least one bit indicating a frequency of the input clock signal.

22. (Previously Amended) A method for performing fast data access in an electronic system including a memory device comprising an array of memory cells, the method comprising:

generating a configuration word incorporating at least one mode select bit and at least one clock frequency indication bit;

loading the configuration word into a mode/configuration register;

generating a delayed clock signal from an input clock signal such that the delay is selected from a plurality of delays in response to the at least one clock frequency indication bit;

selecting between the input clock signal and the delayed clock signal, in response to the at least one mode select bit, to generate a selected clock signal;

generating a plurality of data FIFO register control signals in response to the selected clock signal;

storing a plurality of data bits from the array of memory cells to a data FIFO register; and

accessing the plurality of data bits from the data FIFO register at a rate determined by the plurality of data FIFO register control signals.